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A Variable Gain-CMOS Instrumentation Amplifier: Case Study

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ABSTRACT: In this paper we have designed and implement the variable gain instrumentational amplifier for high frequency application. Front end amplifier required to have a high input impedance through which intended current is measured, signal coming from the tissue of human body is applied to an IA through electrodes, before going for an imaging. So that the signal can be boost up, detectable and immune to noise. For imaging of cancer biomarkers it is necessary to measure bioimpedance over a wide range of frequency 10 KHz to 2 MHz. The circuit is intended for a wideband bioimpedance imaging application, required gain up to 40dB. Other than this it is giving a 100 dB CMRR at the high frequency of 8MHz with low power dissipation of 567 µw, low input referred noise and minimum area of 0.000985 mm-square. This local current feedback variable gain IA is compared with two IA (Current feedback IA and indirect current feedback IA) and is comparatively more stable, higher CMRR value. This amplifier is a boon to bioimpedance imaging, EIT and other bio-medical applications.

KEYWORDS: Cancer biomarkers, CMOS, bioimpedance, high CMRR, instrumentation amplifier (IA), local current feedback, imaging, Electrical Impedence Tomography (EIT), Electro Cardio Graph (ECG).

I. INTRODUCTION

Instrumentation amplifiers (in-amps) amplify the difference between two signals. These differential signals typically emanate from sensors such as resistive bridges or thermocouples.

An instrumentation (or instrumentational) amplifier is a type of differential amplifier that has been outfitted with input buffer amplifiers, which eliminate the need for input impedance matching and thus make the amplifier particularly suitable for use in measurement and test equipment. Additional characteristics include very low DC offset, low drift, low noise, very high open-loop gain, very high common-mode rejection ratio, and very high input impedances. Instrumentation amplifiers are used where great accuracy and stability of the circuit both short and long-term are required.

The specification of common mode rejection ratio (CMRR) is a measure of the extent to which common mode signals are rejected by an amplifier. An instrumentation amplifier is a closed-loop gain block that has a differential input and an output that is single-ended with respect to a reference terminal. Most commonly, the impedances of the two input terminals are balanced and have high values, typically 1000G ohms, or greater. The input bias currents should also be low, typically 1 nA to 50 nA. As with operational amplifiers, output impedance is very low, nominally only a few milliohms, at low frequencies. Unlike an op amp, for which closed-loop gain is determined by external resistors connected between its inverting input and its output, an in-amp employs an internal feedback resistor network that is isolated from its signal input terminals. With the input signal applied across the two differential inputs, gain is either preset internally or is user set (via pins) by an internal or external gain resistor, which is also isolated from the signal inputs.

Application examples include automotive transducers [1], industrial process control [2]-[4], linear position sensing, and biopotential acquisition systems[6]-[11]. Main focus is on the design of integrated instrumentation for medical impedance imaging using bioimpedance measurements [12], [13]. Bioimpedence imaging is also known as electrical impedence tomography which is far better than the other medical imaging techniques. It has advantage over other techniques such as noise free, radiation less, highly portable, and inexpensive. In a bioimpedance imaging system a differential alternating current is applied through a pair of surface electrode to the body tissue and resulting voltages are picked up by another electrode which is further amplified and processed [15]. Amplifier has its necessity of high input

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impedence to avoid the part of produced current into the circuit, which would cause erroneous faults. Thus IA is required. The main focus is on to detect the micro volts (µvolts) differential signal of the body tissue in the presence of milli-volts (mv) common mode interring signal at working frequency of few Hz to MHz.

Common-mode rejection (CMR), the property of cancelling out any signals that are common (the same potential on both inputs), while amplifying any signals that are differential (a potential difference between the inputs), is the most important function of an instrumentation amplifier provides. Both dc and ac common-mode rejection are important in-amp specifications. Any errors due to dc common-mode voltage (i.e., dc voltage present at both inputs) will be reduced 80 dB to 120 dB by any modern in-amp of decent quality. In-amps are widely used in medical equipment such as EKG and EEG monitors, blood pressure monitors, and defibrillators.

II. RELATED WORK

An enhanced current-mode instrumentation amplifier is shown in fig 1. The circuit is based on a current conveyor operational amplifier combined configuration that offers significant improvement in accuracy as compared with the basic current-mode instrumentation amplifier based on current conveyors only.

In Fig 1 It comprises of two op amps working in conjunction with current conveyors. In practice, this circuit will also need a buffered output. Each current conveyor has its input circuit within the negative feedback loop of an op amp. The high loop gain of the op amp ensures that the current through the input resistors Rx at the inverting inputs of the current conveyors is determined solely by the external resistor Rg in conjunction with the differential input voltage. The overall effect of this is Rx that is eliminated from the circuit transfer function.

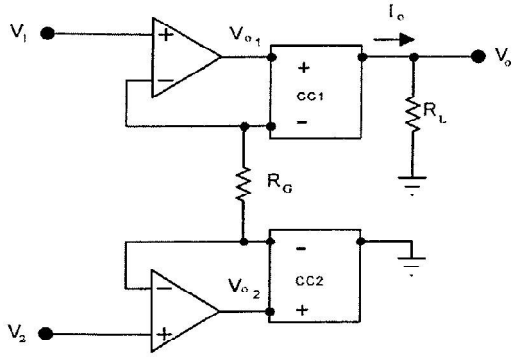

Fig. 1: Current-mode instrumentation amplifier using operational amplifiers and current conveyors.

Fig. 2 shows the simplified circuit schematic of the local current feedback IA [17]. The input transconductor stage uses a simple current mirror load (drain network) and current source biasing (source network). The sensing amplifier serves to exactly balance the drain currents of transistors Mi1 and Mi2 by adjusting the complementary currents I1 and I2. A direct result of this is that the input differential voltage is forced across resistor R1 and hence Mi1 and Mi2 of the input stage essentially acts as a unity-gain buffer.

Similarly, the high gain amplifier B balances the drain currents of transistors Mo1 and Mo2 in the output transconductor stage. Since currents I3 and I4 are exact copies of I1 and I2, respectively, the output voltage V0 appears across resistor R2. Hence, the dc gain of the IA is given by the ratio R2/R1. Placing a capacitor C2 in parallel with resistor R2 creates a dominant pole, which sets the 3 dB BW of the IA.

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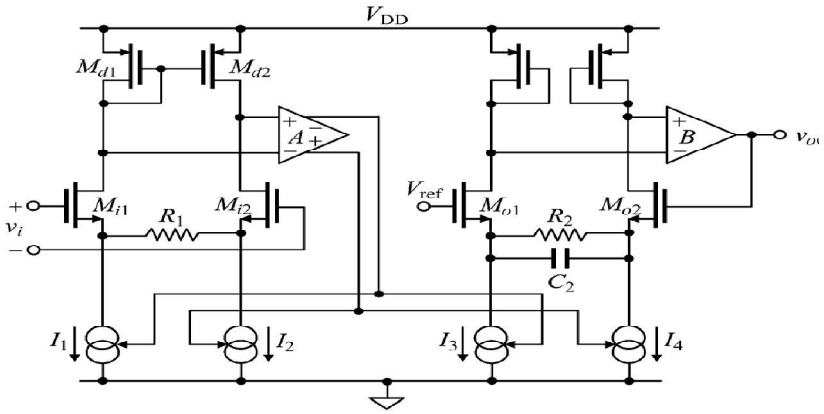

Fig. 2: Simplified model of a instrumentation amplifier with current feedback [17]

The common-mode gain characteristics of the IA due to random mismatches can be analyzed by focusing only on the input stage. This is because the mismatch effects of the sensing amplifier A and the output transcondutance stage are greatly suppressed by the high gain of the local feedback loops. Fig. 2 shows the small-signal model of the IA's input stage where it is assumed that the output conductances of Md1, 2 are much less than their corresponding transconductances. The voltages at the drain terminals, d1 and d2, are sensed by the amplifier A which drives the differential feedback current ifs. The feedback path is via the source terminals s1 and s2. In the figure, gmi1,2 and gds1,2 are respectively the transconductances and drain-source conductances of the input transistors Mi1 and Mi2.gmd1,2 are the transconductances of the drain transistors Md1 and Md2.gs1,2 are the output conductances of the current sources I1 and I2 . All parasitic capacitances are included to allow a study of the high-frequency mismatch characteristics. Cs1,2 and Cd1,2 are respectively the gate-source and gate-drain capacitances of the input transistors Mi1 and Mi2, and Cs1,2 and Cd1,2 are respectively the *total* capacitances of the source and drain terminals, including those from the input and load/source transistors as well as the amplifier stages that are connected to the terminals.

III. BLOCK DIAGRAM OF PROPOSED WORK

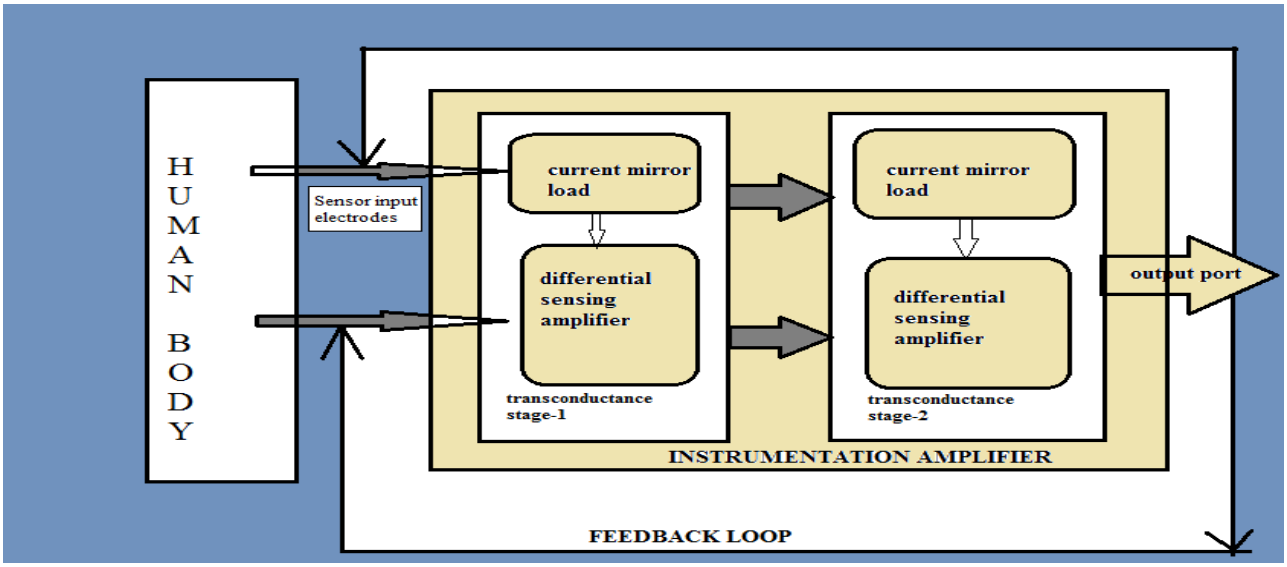

Fig 3: Block diagram of the proposed IA

Fig 3 shows the block diagram of proposed Instrumentation amplifier. Two sensing electrodes are connected to human body through which the change in the potential across two tissues is detected. Front end amplifiers are required

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to detect even micro-voltage signal in the presence of milli-voltage common mode signal; which is a challenging task. So a high input impedance IA is required. Sensing input is fed to a transconducting stage with local current feedback. Local current feedback has various advantages over resistor feedback in terms of balancing and degree of matching.

Both the direct and indirect current feedback IA topologies are subjected to a number of parasitic poles associated with each of the stages around the loop. As a result, this complicates the frequency compensation and poses a limitation on high-frequency operation. On the contrary, in the local current feedback IA topology, each local loop contains a smaller number of internal parasitic poles and thus, this topology potentially offers a higher operating BW for a given current consumption. For these reasons we have chosen the local current feedback IA topology implemented with a current mirror load (drain load) in the input transconductor.

Sensing differential amplifier will sense the small signal and provide it a sufficient gain by matching the drain currents of both the transconductance stages. Current mirror load is provided at each stage to provide better stability by feedback and thus reduced the parasitic. It is also insensitive towards offset voltages where resistive load are sensitive towards offset voltages.

IV. MATHEMATICAL CALCULATIONS OF IA

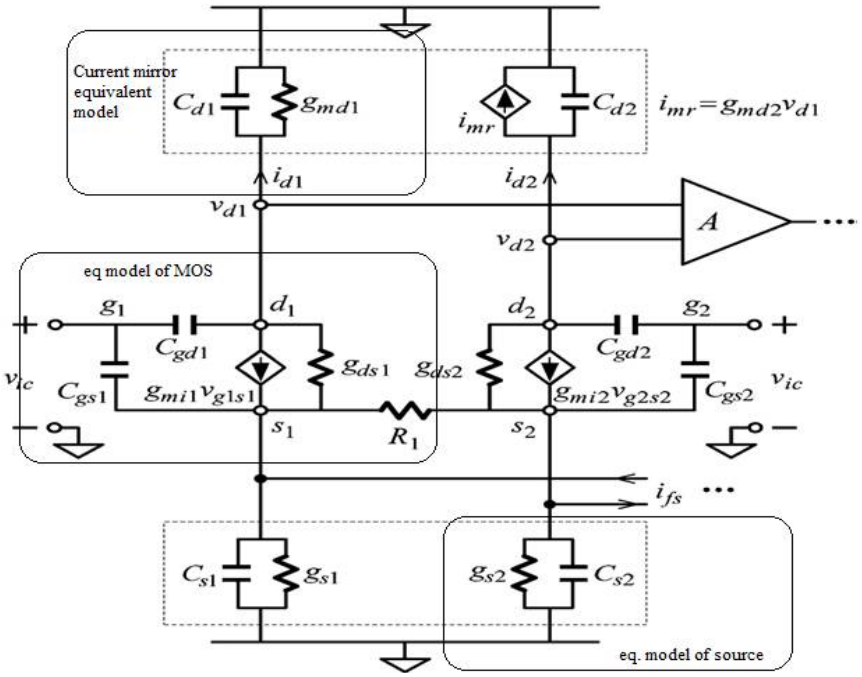

Fig 4: Equivalent model of transconductance stage.

A set of equations governing the common-mode gain characteristics of the IA can be formulated by first applying KCL at the drain and source terminals of the input stage. Next, to obtain the equations for the common-mode signal responses, we take the **sum** between the drain equations at d1 and d2, and between the source equations at s1 and s2. Similarly, to obtain the equation for the differential-mode signal response, we take the **difference** between the drain equations at d1 and d2, and between the source equations at s1 and s2. These sum and difference equations of the KCL node equations enable us to understand the underlying mechanism that leads to a finite common-mode gain due to component mismatches. In particular, the sum equations will be employed to determine the common-mode voltages of the IA. If there are mismatches, the common-mode voltages will give rise to differential current injections into the circuit. Subsequently, the difference equations will be employed to determine the circuit response, and hence the finite common-mode gain of the IA can be computed.

Applying KCL at node s1 in fig 2, we get;

SCs1 * Vs1 + Gs1 * Vs1 + Gmi1 * Vs1 – Gds1 *Vd1 + Gds1 * Vs1 = Gmi1 * Vic1 + SCgs1 * Vic1 .....eq(1)

Applying KCL at node s2 in fig 2, we get;

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SCs2 * Vs2 + Gs2 * Vs2 + Gmi2 * Vs2 – Gds2 * Vd2 + Gds2 * Vs2 = Gmi2 * Vic2 + SCgs2 * Vic2 .....eq(2)

As the two MOSes are identical therefore their internal parameters are also equal. For common mode gain the circuit is open circuited at the midway of R1 resistor . hence removing the suffixes 1 and 2. Adding equation 1 and 2 (also for common mode gain Vs = [Vs1+Vs2]/2) .....eq(3) we get,

2[SCs * Vs + Gs * Vs + Gmi * Vs – Gds * Vd + Gds * Vs] = 2[Gmi * Vic + SCgs * Vic] .....eq(4)
[SCs * Vs + Gs * Vs + Gmi * Vs – Gds * Vd + Gds * Vs] = [Gmi * Vic + SCgs * Vic] .....eq(5)
Taking Vs common from LHS and Vic from RHS;
[SCs + Gs + Gmi – Gds + Gds] * Vs = [Gmi + SCgs] * Vic .....eq(6)

Applying KCL at node d1 in fig2, we get;

Gds1 * Vs1 + Gmi1 * Vs1 – Gmd1 * Vd1 - Gds1 * Vd1 – SCgd1 * Vd1 – SCd1 * Vd1 = Gmi1 * Vic1 – SCgd1 * Vic1 .....eq(7)

Applying KCL at node d2 in fig 2, we get;

Gds2 * Vs2 + Gmi2 * Vs2 – Gmd2 * Vd2 - Gds2 * Vd2 – SCgd2 * Vd2 – SCd2 * Vd2 = Gmi2 * Vic2 – SCgd2 * Vic2 .....eq(8)

As the two MOSes are identical therefore their internal parameters are also equal. For common mode gain the circuit is open circuited at the midway of R1 resistor . hence removing the suffixes 1 and 2. Adding equation 1 and 2 (also for common mode gain Vd = [Vd1+Vd2]/2) .....eq(9) we get,

2[Gds * Vs + Gmi * Vs – Gmd * Vd - Gds * Vd – SCgd * Vd – SCd * Vd] = 2[Gmi * Vic – SCgd * Vic] .....eq(10)

[Gds * Vs + Gmi * Vs – Gmd * Vd - Gds * Vd – SCgd * Vd – SCd * Vd] = [Gmi * Vic – SCgd * Vic].....eq(11)
Taking Vd common from LHS and Vic from RHS;
[Gds + Gmi] * Vs –[Gmd - Gds – SCgd – SCd] * Vd = [Gmi – SCgd]* Vic .....eq(12)

From eq(6) and (12) we get the two unknown and two equation , we can easily calculate Vd and Vs from here and hence common-mode gain.
Now moving towards differential gain we have to consider the in between resistor R1 i.e short circuited , considering dVd = dVd1 – dVd2.....eq(13), dVs = Vs1 – Vs2.....eq(14) and the feedback current Ifs.

Applying KCL at node s1 and s2, we get;

[Gmi * Vs1 + 2/R1 * Vs1 + Gds * Vs1 + Gs * Vs1 + SCgs * Vs1 + SCs * Vs1- Gmi * Vs2 + 2/R1 * Vs2 + Gds * Vs2 + Gs * Vs2 + SCgs * Vs2 + SCs * Vs2]/2 – Gds * (Vd1) + Gds * (Vd2) – Ifs = Gds * (Vd - Vs) – Gmi * (Vic - Vs) + Gs* Vs + SCgs * (Vic - Vs) + SCs* Vs.....eq(15)
From (13) and (14) we get;
(Gmi + 2/R1 + Gds + Gs + SCgs + SCs) * dVs/2 – Gds * (dVd/2) – Ifs = Gds * (Vd - Vs) – Gmi * (Vic - Vs) + Gs* Vs + SCgs * (Vic - Vs) + SCs* Vs.....eq(16)

Applying KCL at node d1 and d2, we get;

[Gmi * Vs1- Gmi * Vs2 + Gds * Vs1 – Gds * Vs2]/2 - [Gds * Vd1 + SCd * Vd1 + SCgd * Vd1 - Gds * Vd2 - SCd * Vd2 + SCgd* Vd2]/2 – Ifd = Gmi (Vic - Vs) + Gds (Vd - Vs) + Gmd * Vd – SCgd * (Vic - Vd) + SCd * Vd.....eq(17)
From eq (13) and (14) we get;
(Gmi + Gds**) *** dVs/2 – (Gds + SCgd + SCd) * dVd/2 – ifd = Gmi (Vic - Vs) + Gds (Vd - Vs) + Gmd * Vd – SCgd * (Vic - Vd) + SCd * Vd.....eq(18)
Hence from equation 16 and 18 we can easily calculate the differential gain. Following this, we have dVd = Vd1-Vd2~0, i.e., a differential-mode virtual ground condition.
Where Gds is the drain-source conductances of the input transistors, Gmi is the transconductance of the input transistor. Cgs and Cgd are respectively the gate-source and gate-drain capacitances of input transistors, Cs and Cd are

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respectively the total capacitances of the source and drain terminals, ifs is the differential feedback current, Gmd is the transconductance of the drain transistors.

V. DESIGNING OF INSTRUMENTATION AMPLIFIERS: ANALYSIS

We have designed three different IA in this paper. Fig 5 shows the direct current feedback instrumentation amplifier. It is often used in low power biomedical applications. Transistors connected to the input terminals and resistors in between them form a voltage to current converter with a transconductance of 1/R1. Another voltage to current converter is formed between bottom two transistor pairs with a transconductance of 1/R2, which provides feedback from the output.

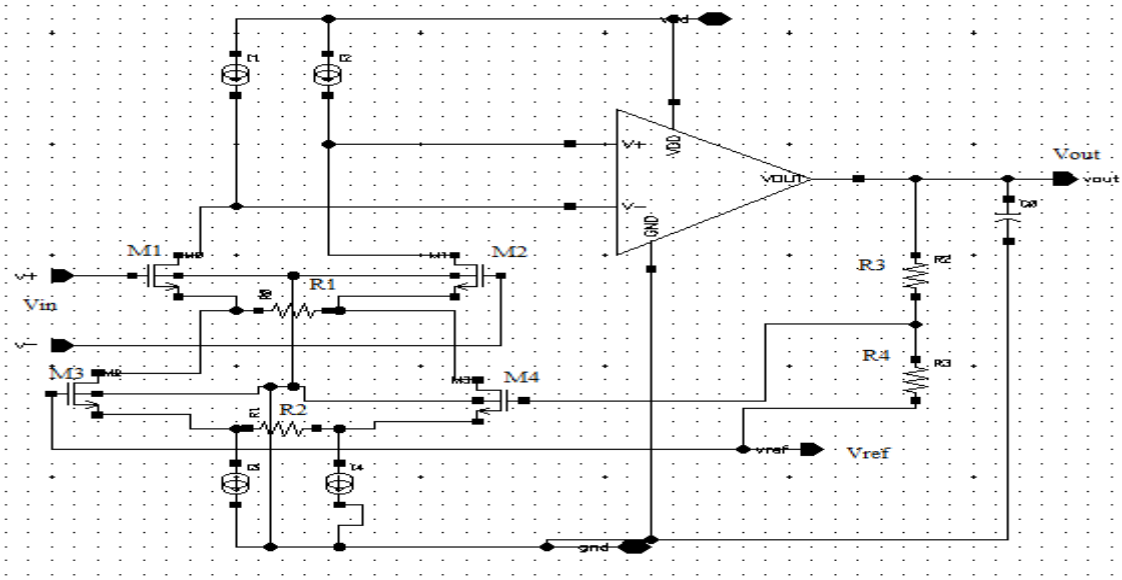

Fig 5: schematic diagram of direct current feedback IA

The gain of the current feedback IA is given by the mathematical expression:
{(Vout-Vref)/Vin} = {(R3 + R4)/R4}(G1/G2) where G1 is the transconductance composed of M1, M2 and R1, G2 is the transconductance composed of M3, M4 and R2. In this circuit M1, M2 are always biased at the same drain current I, while transistors M3, M4 carry a signal dependent drain current. This difference in the bias currents can be a source of nonlinearity. The cascading of two voltage to current converters decreases the input common mode voltage range.

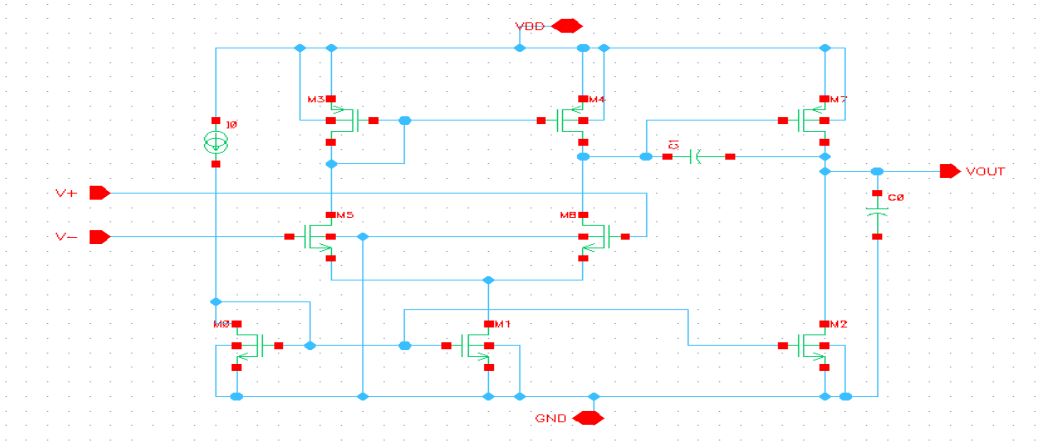

Fig 6: schematic diagram of two stage opamp used in the IA

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Fig 6 shows the schematic diagram of two stage opamp which is used in direct and indirect feedback instrumentation amplifiers to provide large loop gain. 2 stage opamp provides a gain of 50 dB; consists of two capacitors of C0 and C1 where C0 = 8pF and C1 = 3pF. Total of 5 NMOS and 3 PMOS are placed, a dc current source is provided at the current mirror load to maintain the drain current of differential amplifier stage, also at last voltage buffer is used.

Fig 7 shows the indirect current feedback instrumentation amplifier. The gain equation is same as in direct one, {(Vout-Vref)/Vin} = {(R3 + R4)/R4}(G1/G2). In this approach the transistors M1 and M2, M3 and M4 carry a signal dependent drain current, thereby eliminating this source of non-linearity, while the minimum supply voltage and input voltage ranges are also relaxed. Here input common mode voltage and reference common mode voltage are independent with each other. So to achieve this we have to give more current dissipation. Hence it is used where good linearity and gain accuracy is required.

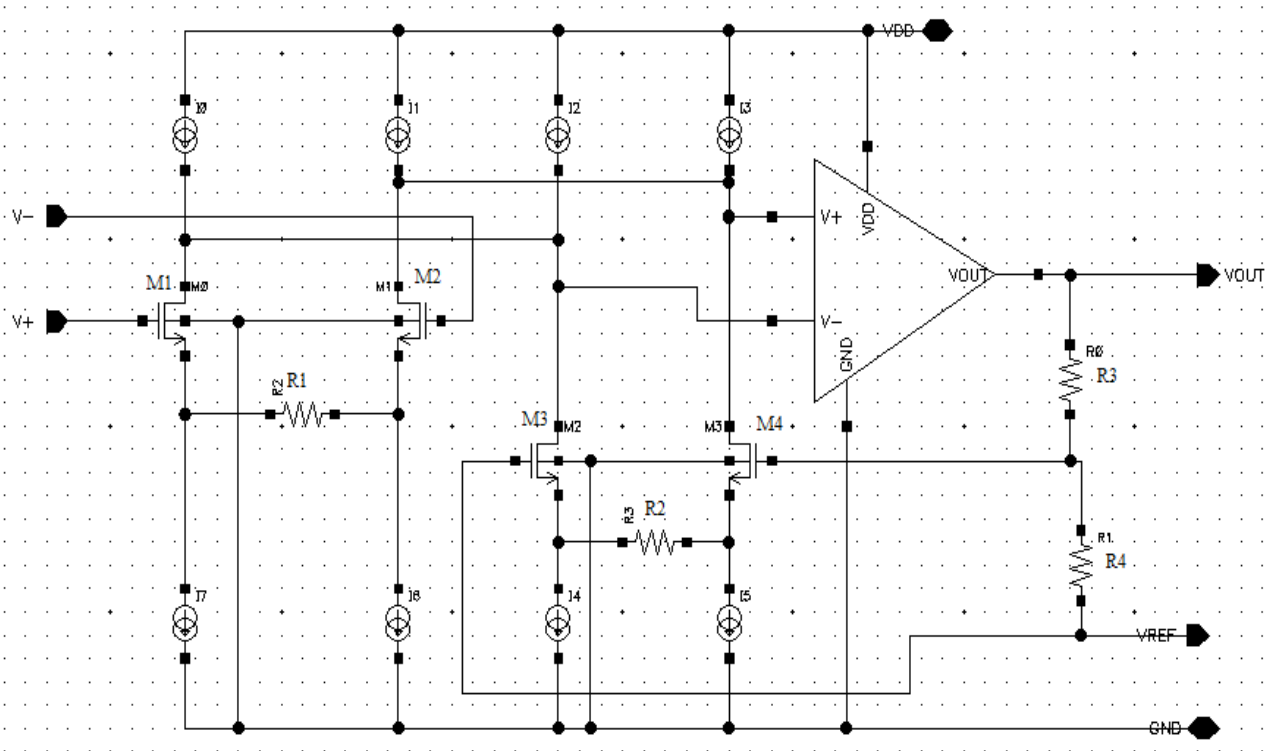

Fig 7: schematic diagram of indirect current feedback IA

Fig 8 & 9 are the schematic of proposed instrumentation amplifier with given specification, sizes of MOS, resistors, capacitors. It is designed in virtuoso design environment, using 180nm technology. Library files included is UMC18CMOS technology files, all the components are placed from the same library files. Three terminal resistors and capacitors are used and 3rd terminal is connected to VDD as body is of P-type. Total of 33 MOS with 10 resistors and 2 capacitors are required with a power supply of 1.8V.

Circuit implementation: Vbias1 = 600mV, Vbias2 = 1 V, Vref = 200 mV, idc = 70micro-amps. Two resistor banks are used to provide the variable gain to the IA. R0 (input resistor) resistor values are taken from 20 to 400 ohms, and R1 (output resistor) resistor values are taken from 10 K too 1M ohms. NMOS transistor is used as a switch to provide ON and OFF switch to particular resistor; it is connected to the voltage supply in order to switch ON or OFF.

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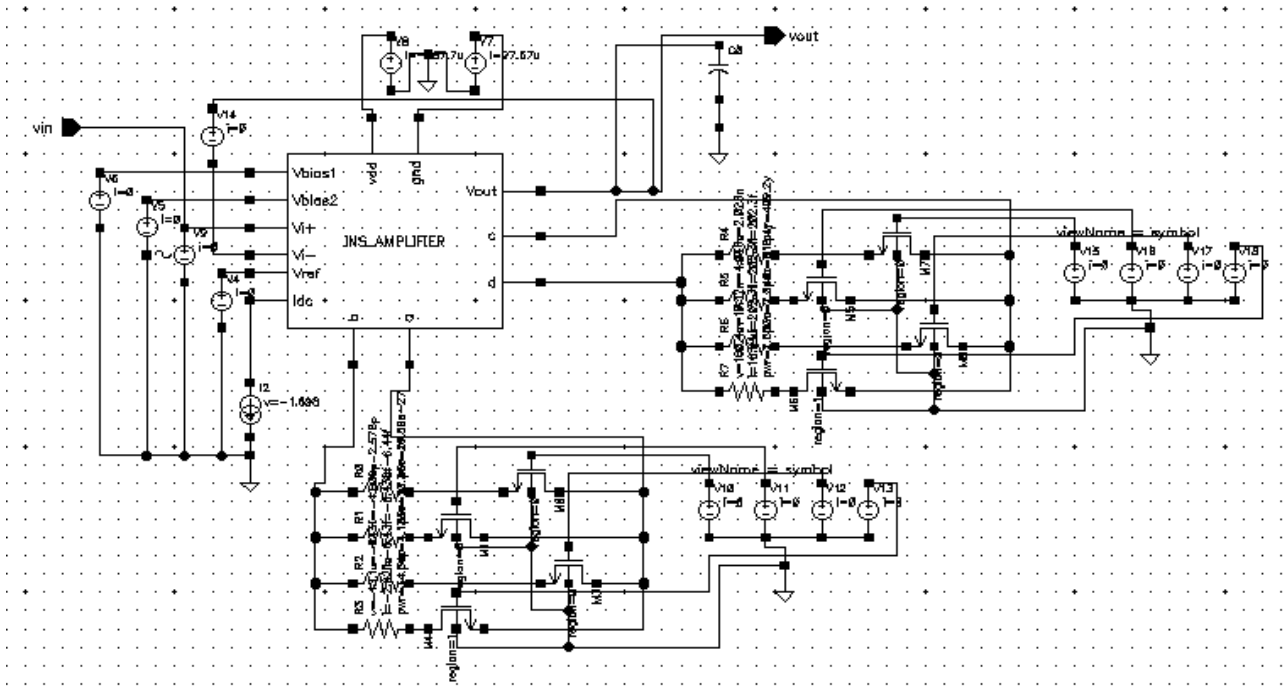

Fig 8: test bench simulation with resistor banks for R0 & R1

There are basically two approaches for designing of an IA. One is resistive feedback {3 opamp circuit of IA [11]} and second approach is current feedback [16]. Here we are using current feedback because of few reasons and disadvantages of resistive feedback circuits like CMRR is reduced by degree of matching of the resistors but in current feedback there is perfect isolation between input and output and balancing technique is also achieved.

In local current feedback IA there are few number of internal parasitic poles and thus this circuit offers a higher 3dB frequency and operating bandwidth. While in case of other feedback such as direct and indirect feedback [4] there are more number of poles associated with each stage and hence operating bandwidth reduces. Fig 1 current feedback is implemented with current mirror load transconductor [7]. One positive point of current mirror is insensitive to input offset voltage of loop amplifier. It also provides a large loop gain due to its higher impedence output node.

Ultimately sensing amplifier has relatively low gain and which will provide better stability, high bandwidth, hence power-area efficient.

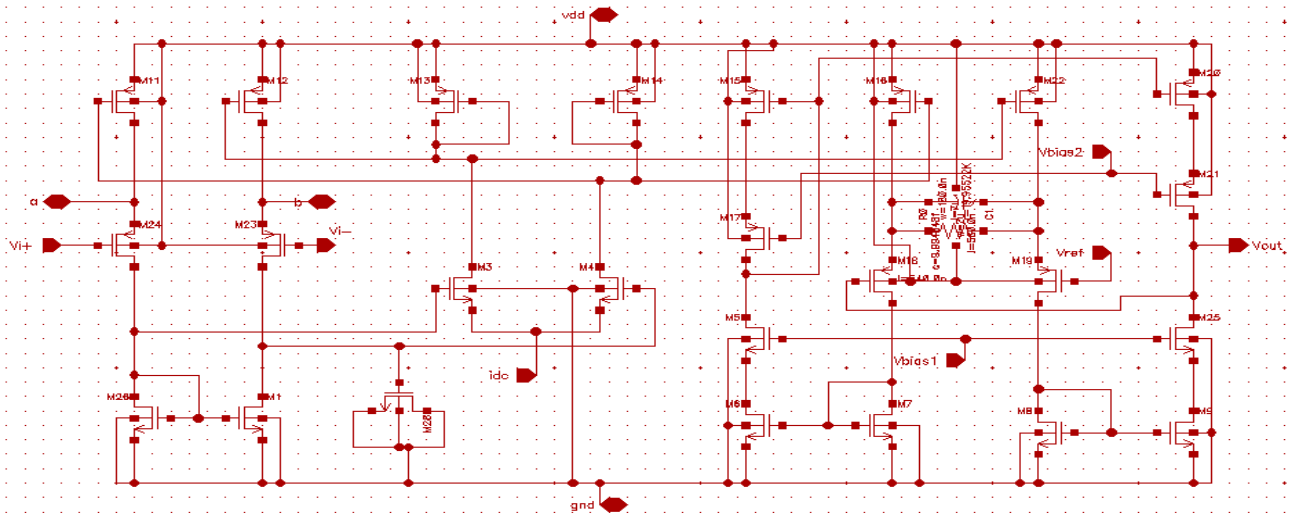

Fig 9: schematic diagram of proposed IA

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Table 1: UMC18_CMOS technology components used

S.NO	MOS USED	DRAIN CURRENT	REGION OF OPERATION	W/L RATIO
1.	M1 NMOS	56.74µA	2(SATURATION)	2µm/180nm
2.	M2 NMOS	22.06µA	2	540nm/180nm
3.	M3 NMOS	75.01µA	2	3µm/180nm
4.	M4 NMOS	14.99µA	2	3µm/180nm
5.	M5 NMOS	1.79µA	2	240nm/240nm
6.	M6 NMOS	1.79µA	2	240nm/540nm
7.	M7 NMOS	1.55µA	2	240nm/540nm
8.	M8 NMOS	18µA	2	2µm/180nm
9.	M9 NMOS	10.37µA	2	500nm/180nm
10.	M2B NMOS(capacitor)	0A(Shorted)	1(LINEAR)	240nm/180nm
11.	M11 PMOS	-13.33µA	2	10µm/180nm
12.	M12 PMOS	-13.33µA	2	10µm/180nm
13.	M13 PMOS	-75.07µA	2	10µm/180nm
14.	M14 PMOS	-1.79µA	2	10µm/180nm
15.	M15 PMOS	-1.79µA	2	1µm/180nm
16.	M16 PMOS	-12.34µA	2	10µm/180nm
17.	M17 PMOS	-1.79µA	2	240nm/180nm
18.	M18 PMOS	-1.55µA	1	240nm/540nm
19.	M19 PMOS	-18µA	1	1µm/180nm
20.	M20 PMOS	-10.37µA	2	5µm/180nm
21.	M21 PMOS	-10.37µA	2	5µm/180nm
22.	M22 PMOS	-5.41µA	2	1µm/180nm
23.	M23 PMOS	-58.74µA	1	5µm/180nm
24.	M24 PMOS	-22.06µA	1	5µm/180nm
25.	M25 NMOS	10.37µA	2	540nm/180nm

VI. SIMULATED RESULTS OF IA

CMRR is defined as the ratio of differential gain to common mode gain. (CMRR = Ad/Ac), fig 10 shows Ad and Ac but they are in dB so we have to use logarithms identity rules here. Therefore CMRR = Ad-[-Ac]

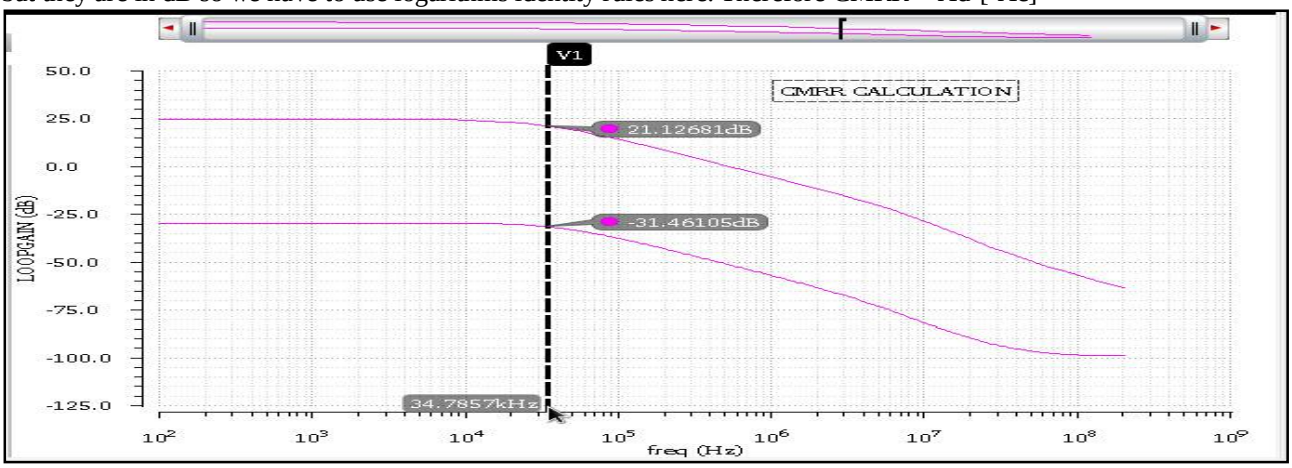

Fig 10: CMRR analysis and bandwidth of direct feedback IA

From fig 10 CMRR at 34.7857 KHz cut-off frequency = 21.12-[-31.46]. Hence CMRR = 52.58 dB, which is comparatively low for a imaging amplifier. In order to achieve a high rejection over common mode signals CMRR should be above 80 dB. However power dissipation for this IA is minimum (222 micro-watts); hence it is used in low power applications where low power is the fundamental aim of the device.

The **common-mode rejection ratio** (CMRR) of a differential amplifier (or other device) measures the ability of the device to reject common-mode signals, those that appear simultaneously and in-phase on both amplifier inputs. An ideal differential amplifier would have infinite CMRR; this is not achievable in practice. A high CMRR is required when a differential signal must be amplified in the presence of a possibly large common-mode input. The CMRR is a very important specification, as it indicates how much of the common-mode signal will appear in your measurement.

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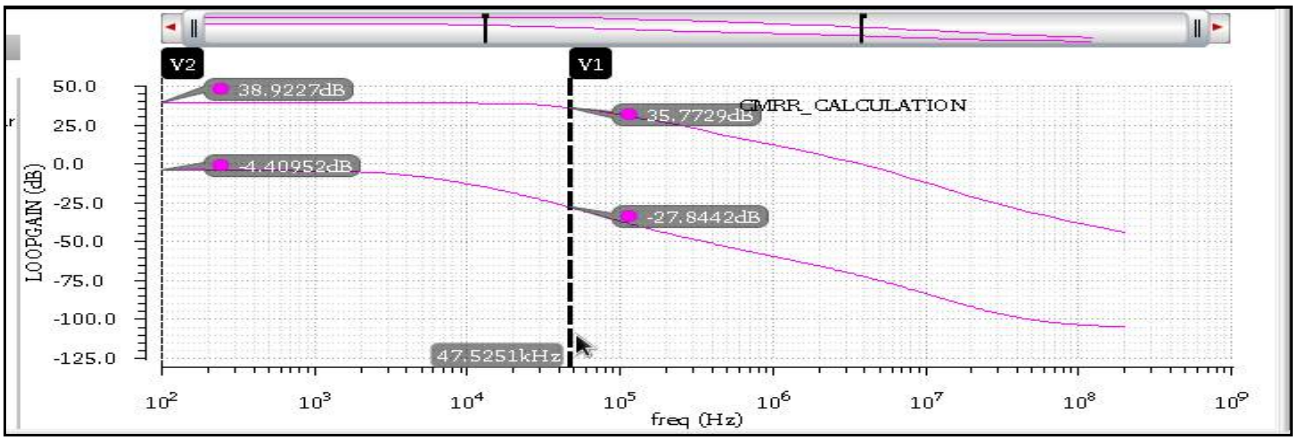

Fig 11: CMRR analysis and bandwidth of indirect feedback IA

Fig11 shows CMRR at 47.52 KHz cut-off frequency = 35.77-[-27.844]. Hence CMRR = 63.614 dB, which is also comparatively low for an imaging amplifier. In order to achieve a high rejection over common mode signals CMRR should be above 80 dB. Fig 12 shows CMRR analysis of the proposed IA at R0 = 400 ohms and R1 = 20 K ohms and cut-off frequency of 8 MHz.

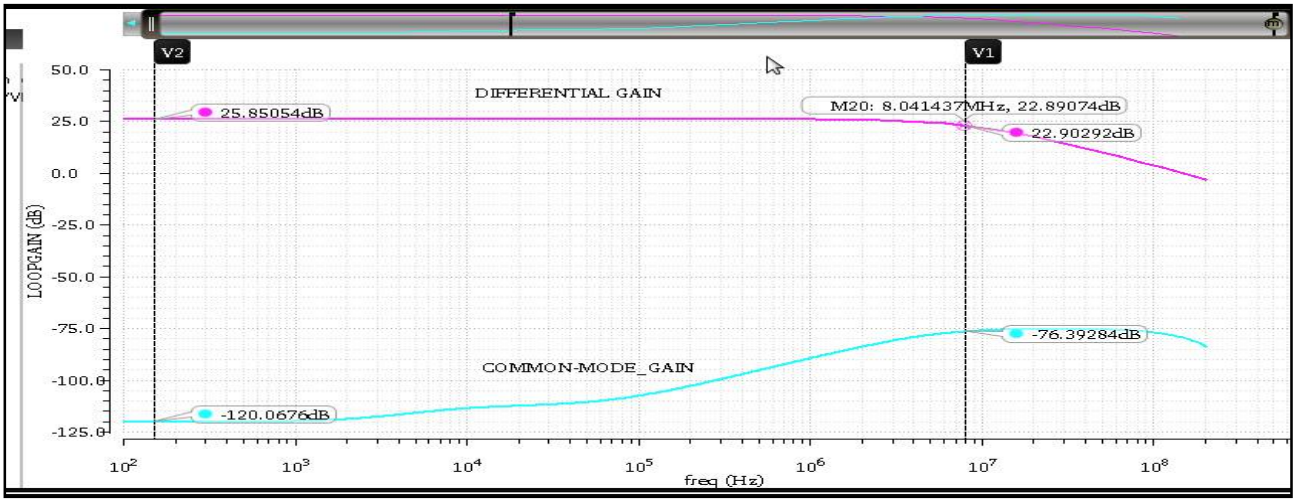

Fig 12: CMRR analysis and bandwidth of proposed variable-gain IA

Calculating CMRR from fig 12 we get, CMRR at 8 MHz cut-off frequency = 22.90-[-76.39]. Hence CMRR = 99.29 dB which is excellent at this frequency (which is our target result). At low frequency we are getting 145.85 dB and this is strong rejection to common mode noise. Detection of small signals from tissues in presence of high common mode signals is a challenging task and with this CMRR it is easily gettable. On comparing with above two results we are getting an excellent CMRR at high frequency of 8MHz.

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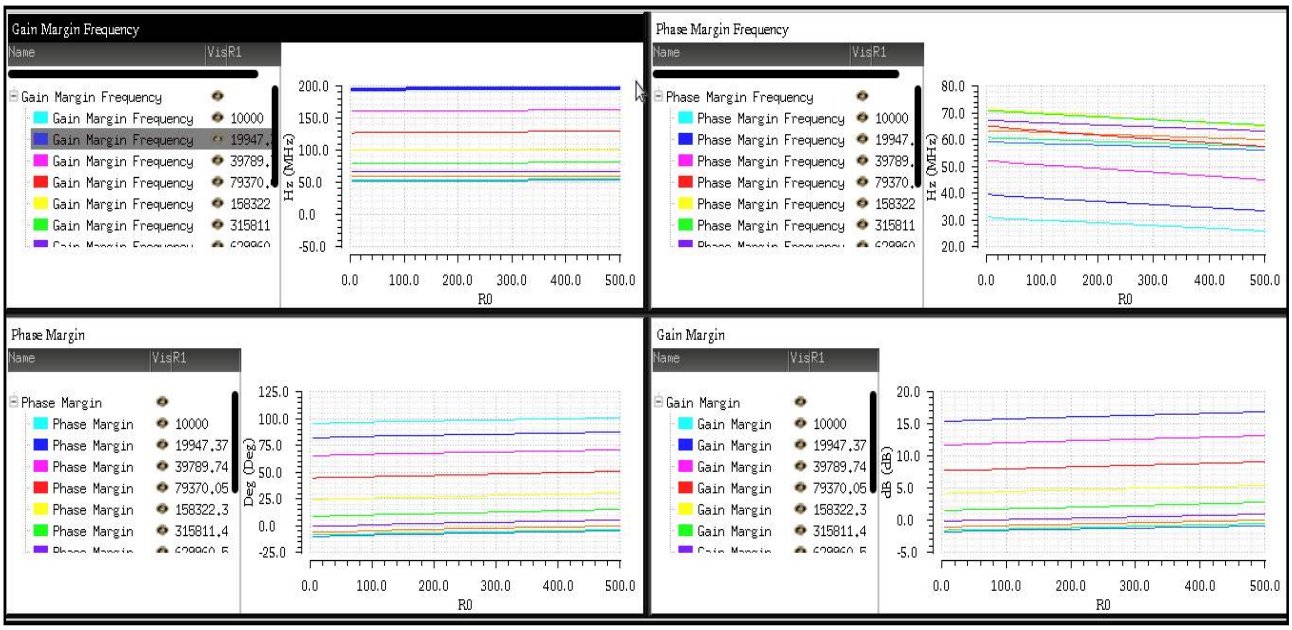

Fig 13: stability summary of the proposed variable-gain IA

Hence, gain of the IA would be the same as earlier one at higher temperature ranges also. This is a necessity of the circuit to be fabricated, which will provide better stability to the amplifiers that are going to work in noisy and tough conditions. Fig 13 shows the stability criterion in terms of frequency response, where **gain margin and phase margin** should be positive. Above 5 dB of GM and for the PM of above 10 degree, the system will be stable. From the figure it can be conclude that for different R0 and R1 values; Wpc(phase cross-over frequency) > Wgc(gain cross-over frequency) and GM,PM are positive that indicates the system is stable enough, provided the loop gain should be high, MOS transistors operates in saturation region and bandwidth of the IA is enough for the requirement of operation. Graph clearly shows that for which value of R0 and R1 the system is unstable (That is GM & PM is negative).

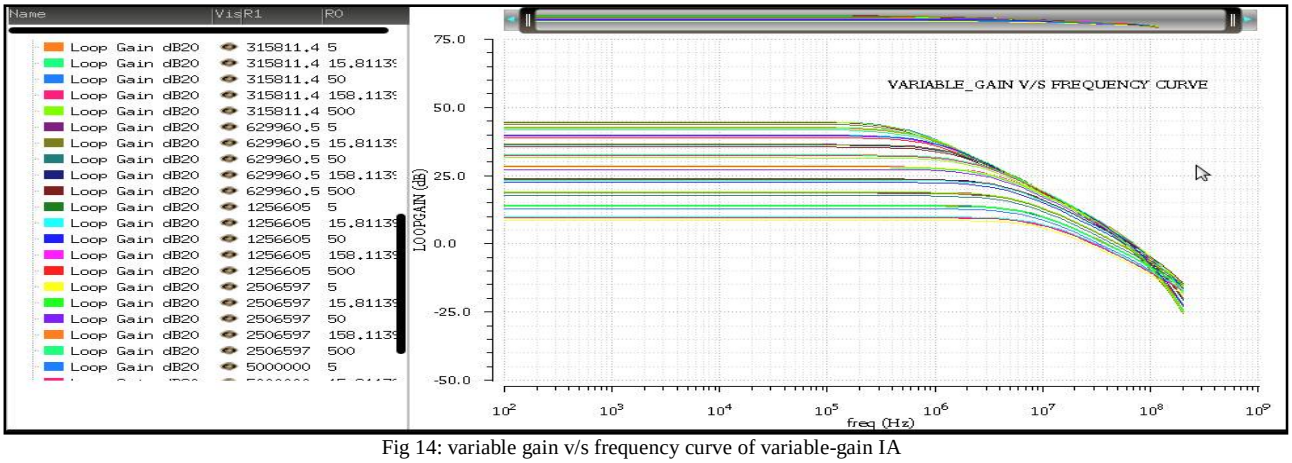

Fig 14: variable gain v/s frequency curve of variable-gain IA

Fig 14 Shows the variation of gain for the different values of resistor R0 (from 20 to 500 ohms with step size = 5) and capacitor C1 (from 1pF to 10 pF with step size of 5) and variable output resistance (R1) from 10K to 1M Ohms So within this region the IA is stable i.e from 15 to 45 dB which is good enough for detecting the small signals. The above graph clearly shows for lower values of R1, the gain is more but we have to trade off between gain and stability here. Thus we cannot reduce R1 below 100 ohm .The speed of the device should always be high enough to give quick

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response. Its slew rate should be infinite ideally. Slew rate is defined as the ratio of change in output voltage with respect to time. Here it is 38.3V/µS.

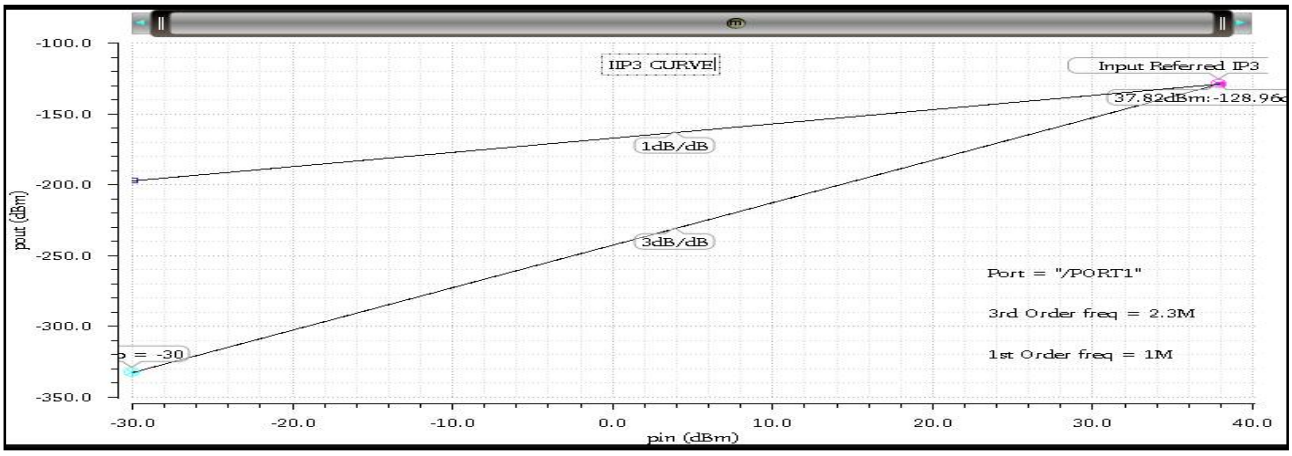

Fig 15: IIP3 analysis of the proposed variable-gain IA

For good linearity, the maximum differential input ranges is restricted to the value 2*Is*R1. Where current here is drain current of source transistor 22.04µA, voltage is therefore 2.2mv and above this harmonic distortion may occur. IIP3 analysis is also shown below fig 15 of 37.93dBm which is good enough. Hence high degree of linearity is obtained.

The intercept point is obtained graphically by plotting the output power versus the input power both on logarithmic scales (e.g., decibels) shown in fig 15. Two curves are drawn; one for the linearly amplified signal at an input tone frequency, one for a nonlinear product. Both curves are extended with straight lines of slope 1 and n (3 for a third-order intercept point). The point where the curves intersect is the intercept point. It can be read off from the input or output power axis, leading to input or output intercept point, respectively (IIP3/OIP3).

When comparing systems or devices for linearity, then, a higher intercept point is better. This device with an **input-referred third-order intercept point** of 37.82dBm is driven with a test signal of −30 dBm. This power is 67.82 dB below the intercept point; therefore nonlinear products will appear at approximately 2x67.82 dB below the test signal power at the device output (in other words, 3×67.82 dB below the output-referred third-order intercept point).

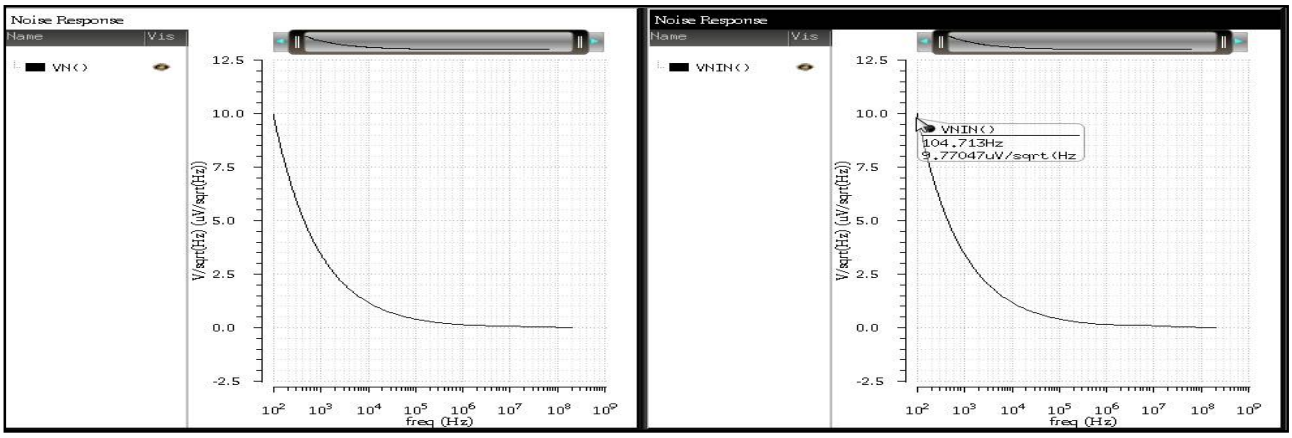

Fig 16: noise response of input and output ports of proposed IA

Fig 16 shows the noise analysis at the input and output ports of the proposed variable gain instrumentation amplifier, which comes out to be 9.77µV/sq-Hz at both input and output ports. Noise occurred in the circuit is due to **shot noise**: the electrons are discrete and are not moving in a continuous steady flow, so the current is randomly fluctuating. **Thermal noise:** caused by the rapid and random motion of electrons within a conductor due to thermal agitation. Both are often stationary and have a zero-mean **Gaussian distribution** (following from the central limit theorem). Here

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noise effect is low at both the ports; hence we can neglect its effect easily in the results. There is circuit noise internal to the subcomponents in the front end. This noise will add on to the AWGN, cause interference, and further degrade the SNR. Circuit noise is associated with the electrical components that build the subcomponents, such as resistors and MOS transistors.

Fig 17 is the **layout** of IA with minimum area with no DRC errors. Resistors are placed apart from power supply in order to achieve low mismatches and minimum resistive layers are used with proper design rules specifications. As circuit designers we must carefully consider how to draw layout for critical/sensitive parts of the circuit in order to get robust and predictable performance.

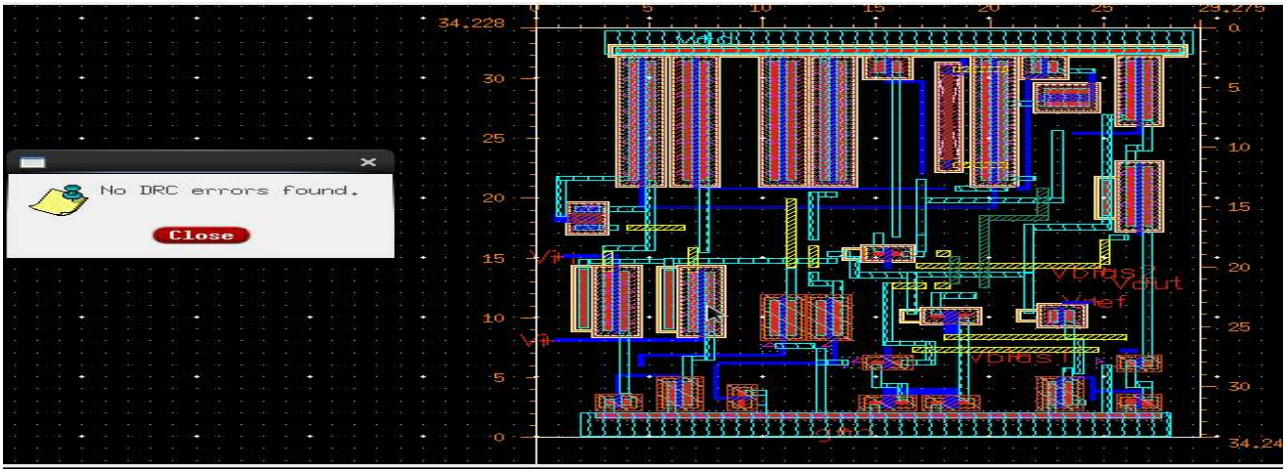

Fig 17: Layout of the proposed variable gain IA

Table 2: CMRR summary of instrumentation amplifiers at their cutoff frequencies

S.NO	INSTRUMENTATION AMPS	COMMON-MODE GAIN	DIFF.GAIN	CMRR
01.	Direct current feedback IA	-30 dB	25 dB	55 dB
02.	Indirect current feedback IA	-27 dB	36 dB	63 dB
03.	Variable gain IA(local current feedback)	-76 dB	24 dB	100 dB

Table 3: Results of proposed variable gain IA

S.NO	PARAMETERS	SPECIFICATIONS	RESULTS OBTAINED
1.	Process technology	-	180nm technology
2.	CMRR	>80 dB at 2MHz	100dB at 8.03MHz
3.	Differential gain	>30 dB	15-45 dB
4.	Common-mode gain	-	-76 dB at 8.03MHz
5.	Slew Rate	>2V/µS	38.3V/µS
6.	Area	Minimum as possible	0.000985mm-sq
7.	Power dissipation	<1mw	567µw
8.	Bandwidth	~2 to 10 MHz	8.03 MHz
9.	Supply voltage	1.8V	1.8V
10.	Input referred noise	<20µV	9.77µV
11.	Gain Margin	Should be positive	>5 dB
12.	Phase Margin	Should be positive	>10 degrees
13.	Wgc	-	Varies as per diff. gain
14.	Wpc	-	Varies as per diff. gain

VII. CONCLUSION AND FUTURE WORK

We have presented a variable gain amplifier with two resistor banks, which will provide variable gain to the IA. Different values of R0 and R1 are considered to obtain the variable gain from 15 to 50 dB. Stability criterion is kept in mind while designing a high bandwidth IA of 8MHz. It gives the information about the stability of the circuit. With varying gain we have to trade off between gain and stability. Other than this it is giving a 100 dB CMRR at the high

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frequency of 8MHz with low power dissipation of 567 μw, low input referred noise and minimum area of 0.000985 mm-square. This local current feedback variable gain IA is compared with two IA (Current feedback IA and indirect current feedback IA) and is comparatively more stable, higher CMRR value. This amplifier is a boon to bioimpedance imaging, EIT and other bio-medical applications.

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